Thesis Defense

Computer Science Master's Program

"Griddle: A novel hardware based matrix multiplier architecture"

By **Seth Kiefer**

Abstract:

Matrix multiplication is a computational cornerstone in modern artificial intelligence and scientific computing, yet general-purpose processors struggle to perform these operations efficiently at scale. This thesis presents Griddle, a novel hardware architecture for matrix multiplication implemented on a Xilinx Artix-7 FPGA. Griddle focuses on flexibility and scalability by adopting a purely iterative approach that supports arbitrarily shaped input matrices without requiring padding or strict dimensional constraints. The architecture uses computational pipelines to execute a multiplication operation. Each pipe consists of a multiplication core and accumulation buffer that compute matrix products in parallel. The multiplication core contains a set of multiplier units which are able to index through the input matrices and compute multiplication operations. The accumulation buffer implements a modified reduction algorithm in order to accumulate multiplication results into a final output cell value. The system's modular design allows configuration of the number of pipelines, multiplier units, and buffer sizes to match available hardware resources. The design was implemented in SystemVerilog and validated through both simulation and implementation on FPGA. Griddle demonstrates a path toward more flexible and adaptable hardware acceleration for matrix multiplication, allowing for reductions in wasted compute potential.

Date: Tuesday, May 27th, 2025
Time: 8:30 AM – 10:30 AM
Zoom: https://calpoly.zoom.us/j/86852198626
Committee: Dr. Danowitz, Dr. Oliver, and Dr. Beard