

“Demystifying Hardware Formal Verification for Undergraduate Education: A RISC-V Processor Case Study with Coursework Implementation”

By Riley Peters

Abstract:

Hardware verification engineers apply formal methods to prove that a digital device always behaves according to its specification. This differs from traditional functional verification, in which engineers establish correctness by repeatedly sending test inputs to the device and comparing the outputs against a reference model. With the growing complexity of integrated circuits, the demand for digital verification engineers with formal methods experience has continued to increase. However, California Polytechnic State University: San Luis Obispo's current curriculum lacks dedicated material to prepare students for these roles.

This thesis seeks to address the lack of formal methods material through two efforts. First, formal and functional verification techniques are applied to two educational RISC-V processors. These case studies demonstrate that applying open-source formal methods tooling is achievable for undergraduates and provides greater functional coverage than simple simulation testing. Building from these cases, this thesis contributes a pair of formal verification workshops that could be integrated into future courses. A preliminary run of the coursework validated its effectiveness in conveying formal verification concepts and helped address remaining flaws in the material.

Date: Friday, March 13th, 2026

Time: 10:30 AM – 12:30 PM

Location: 14-238b

Committee: Dr. Stephen Beard, Dr. John Oliver, Dr. Andrew Danowitz